



Figure 1 Photo of Actual TECA1-XV-XV-D

FEATURES

- High Efficiency: $\geq 90\%$
- Maximum Output Current: 2.5A
- Actual Object Temperature Monitoring
- High Stability: 0.01°C
- High Reliability
- Zero EMI
- Compact Size

DESCRIPTION

The TECA1-XV-XV-D is an electronic module designed for driving TECs (Thermo-Electric Coolers) with high stability in regulating the object temperature, high energy efficiency, zero EMI, and small package. Figure 1 is the photo of an actual TECA1-XV-XV-D TEC controller.

This module provides interface ports for users to set the desired object temperature, i.e. set-point temperature; the maximum output voltage across TEC; and the compensation network. The compensation network compensates the high order thermal load and thus stabilizes the temperature control loop.

It provides these functions: thermistor T-R curve linearization, temperature measurement and monitoring, temperature control loop status indication, TEC voltage monitoring, power up delay, and shut down.

The TECA1-XV-XV-D comes with a high stability low noise 3.0V voltage reference which can be used for setting the desired object temperature by using a POT

(Potentiometer) or a DAC (Digital to Analog Converter). When using this reference for setting the set-point temperature, the set-point temperature error is independent of this reference voltage. This is because the internal temperature measurement network also uses this voltage as the reference, the errors in setting the temperature and measuring the temperature cancel with each other, setting the object temperature with higher stability. This reference can also be utilized by an ADC (Analog to Digital Converter), for the same reason, the measurement error will also be independent of the reference voltage, resulting in a more accurate measurement.

Figure 2 is the real size top view of the controller showing the pin names and locations. The functions of all the pins are shown in Table 1.

The TECA1-XV-XV-D is packaged in a 6 sided metal enclosure, which blocks EMIs (Electro-Magnetic Interferences) to prevent the controller and other electronics from interfering with each other.

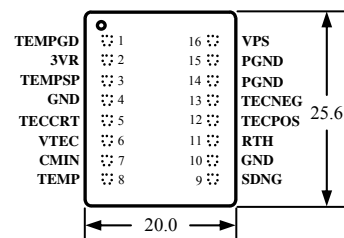


Figure 2 Pin names and Locations

The TECA1-XV-XV-D TEC controller can come with an internal compensation network for stabilizing the temperature control loop. The compensation network with the default values shown in Figure 4 matches most of the commonly used butterfly packaged TEC thermal loads. The part number TECA1LD-XV-XV-D, with the “LD” suffix, stands for the controller with an internal compensation network; while the part number TECA1-XV-XV-D, without the “LD” suffix, stands for the controller without the internal compensation network and external compensation network will be required for the controller to operate. The compensation network is made of 5 components: 3 resistors and 2 capacitors. This network can be implemented either internally by embedding them into the controller circuitries inside the controller enclosure or externally by soldering the 5 components on the PCB (Printed Circuit Board) on which the TEC controller is mounted. Implementing the network externally is highly recommended since it can be modified for driving different thermal load and/or the thermal load characteristics is not certain or fixed at the early design stage. The part number TECA1LD-XV-XV-D denotes the controller with an internal compensation network, the values of the components in the network are either the default values shown in Figure 4 or the values specified in the part number, the naming rules are shown in Table 3.



SPECIFICATIONS

Table 1 Pin Function Descriptions

Pin #	Pin Name	Type	Description
1	TEMPGD	Digital output	Temperature good indication. It is pulled high when the set-point temperature and the actual desired object temperature are $<0.1^{\circ}\text{C}$ in temperature difference when the set-point temperature range is 20°C ; or $<3\text{mV}$ in voltage difference between the voltages of TEMP and TEMPSP nodes. On this pin, there is an internal pull up resistor of 10K tied to the VPS rail. When going low, this pin is pulled down by an open drain FET with a resistance of $250\Omega @ \text{VPS} = 5\text{V}$ or $350\Omega @ \text{VPS} = 3.3\text{V}$.
2	3VR	Analog output	Reference voltage output, 3V. It can be used by a POT or DAC for setting the set-point temperature voltage on the TEMPSP pin and/or a DAC for measuring the temperature through the TEMP pin. The maximum sourcing current capability is 1.5mA and the maximum sinking is 4mA with a stability of $<50\text{ppm}/^{\circ}\text{C}$ max.
3	TEMPSP	Analog input	Object set-point temperature input port. It is internally tied by a 50K resistor to the half value of the reference voltage, 1.5V. The open circuit voltage of this pin is thus 1.5V, corresponding to a set-point temperature of 25°C by using the default temperature network (with the set-point temperature range being from 15°C to 35°C). It is highly recommended to set this pin's voltage by using the controller's voltage reference. The lower limit of the setting voltage for this pin is 0.1V. Setting this pin to a $<0.1\text{V}$ voltage may cause the controller over cooling the object. This pin can also be set to a voltage that is about 0.2V away from the VPS rail. For example, when $\text{VPS} = 5\text{V}$, this pin can be set up to 4.8V, corresponding to approximately 50°C in temperature when the default temperature network is in place, see the curve shown in Figure 6. This pin can be set by using a POT or DAC. When the set-point temperature needs to be at 25°C , leave this pin unconnected.
4	GND	Ground	Signal ground for the POT, ADC, DAC and the thermistor, see Figure 4.
5	TECCRT	Both analog input and output	TEC control voltage. It can be left unconnected or used to control the TEC voltage directly. Set TECCRT between 0V to VPS, the voltage across TEC will be: $\text{TEC voltage} = 2 \times \text{TECCRT} / \text{VPS}$. It can also be used to configure the maximum voltage cross the TEC: $\text{Max. TEC voltage} = V_{\text{TEC_Max}} \times R_m / (R_m + 10\text{K})$, where $V_{\text{TEC_Max}}$ is the maximum output voltage of the TEC controller configured by the internal limiting circuit when the controller is released by the factory, it is marked on the TEC controller label; R_m is the resistance of the two resistors one between TECCRT to GND and the other between TECCRT to VPS, as shown in Figure 4. When the resistor R_m 's are in place or the TECCRT pin is used for controlling the TEC voltage directly, this pin can be utilized for monitoring the voltage across the TEC: $\text{TEC voltage} = (\text{max. TEC voltage}) \times (1 - 2 \times \text{TECCRT}/\text{VPS})$. The output impedance of this pin is 5K.
6	VTEC	Analog output	TEC voltage indication. When the R_m 's mentioned above or the TECCRT is not used for controlling the output TEC voltage directly, this pin can be utilized for monitoring the output voltage across the TEC: $\text{TEC voltage} = (\text{max. TEC voltage}) \times (1 - 2 \times \text{VTEC}/\text{VPS})$. The maximum driving current of this pin is 30mA and the output voltage swing is 0V to VPS.
7	CMIN	Analog input	Compensation input pin for the thermal control loop. Connect the compensation network to this pin as shown in Figure 4 or leave it unconnected if the TEC controller has an internal compensation network already. This pin is noise sensitive. Do not connect this pin with a long wire in the air or long trace on the PCB when layout the board for the TEC controller.



8	TEMP	Analog output	Actual object temperature indication. It swings from 0V to VPS. By a default internal temperature network, it represents 15°C to 35°C when this pin's voltage swings 0V to 3V linearly; when changing from 0V to 5V, it represents 15°C to 50°C in temperature, see Figure 6.
9	SDNG	Digital input	Shut down control. When pulled low, it shuts down the controller. Leave it open or pull it high to activate the controller. This pin is internal pull up by a resistor of 100K to VPS. The threshold voltages of this pin are: before shuts down, the quiescent current is about 45mA; when going down, SDNG = 1.36V shuts down the TECNEG output stage and the quiescent current becomes 26mA; SDNG = 0.8V shuts down TECPOS output stage and the quiescent current becomes 10mA; when going up, SDNG = 1.0V activate the TECPOS output stage and the quiescent current goes back to 26mA; SDNG = 1.37V activates the TECNEG output stage and the quiescent current goes back to the full normal value of 45mA. The maximum input voltage range allowed on this pin is from 0V to 6V.
10	GND	ground	Signal ground, internally connected to Pin 4 GND. It can be used for connecting the return pass of the thermistor.
11	RTH	Analog input	Connect to the thermistor for sensing the object temperature. By using the default temperature network that comes with the standard TEC controller, the thermistor is expected to have a 10K Ω @ 25°C and the R-T curve data are give in Figure 5. The β value of the thermistor is 3170.1. Other thermistors or temperature sensors can also be used, other set-point temperature range can also be set, consult with us.
12	TECPOS	Analog power output	Connects to TEC positive terminal
13	TECNEG	Analog power output	Connects to TEC negative terminal
14	PGND	Power ground	Power ground for connecting to the power supply
15	PGND	Power ground	Power ground for connecting to the power supply, internally connected with pin 14
16	VPS	Power input	Positive power supply rail. Two possible values: 3.3V and 5V, depending on the module.

Table 2 Characteristic ($T_{\text{ambient}}=25^{\circ}\text{C}$)

Parameter	Test Condition	Value	Unit/Note
Object* temp. stability vs. ambient temp	VPS = 5V, $R_{\text{load}} = 2\Omega$	0.0002	$^{\circ}\text{C}/^{\circ}\text{C}$
Offset Object temp. vs. set-point temperature	T_{ambient} is 0~50°C, set-point temp. is 15°C ~35°C	± 0.1	$^{\circ}\text{C}$
Object temp. response time	≤ 0.1 to the set-point temperature at a 1°C step	<5S	S
Efficiency	VPS = 5V, $R_{\text{load}} = 2\Omega$	$\geq 90\%$	-
Max. output current	VPS = 5V, $R_{\text{load}} = 2\Omega$	2.5	A
Max. output voltage	VPS = 5V, $R_{\text{load}} = 2\Omega$	0 ~ (VPS - 0.2)	V
Power supply voltage	—	3.1 ~ 3.5 or 4.75 ~ 5.25 (specify 3.3 or 5)	V
Set-point temp.** control voltage	VPS = 5V, $R_{\text{load}} = 2\Omega$	0.1 ~ VPS	V
Default set-point temp. range***	VPS=3V	15 ~ 35	$^{\circ}\text{C}$
Operating ambient temp. range	VPS = 5V, $R_{\text{load}} = 2\Omega$	-25 ~ 85	$^{\circ}\text{C}$

* Object temperature refers to the actual temperature of the object which is mounted on the cold side the TEC and its temperature needs to be regulated by the TEC. This object is often a metal block on which a laser diode or an optical crystal is mounted.

** Set-point temperature is the temperature of the object desired to achieve.

*** Can be customized to any range according to requirement.

BLOCK DIAGRAM

The block diagram of the controller is shown in Figure 3.

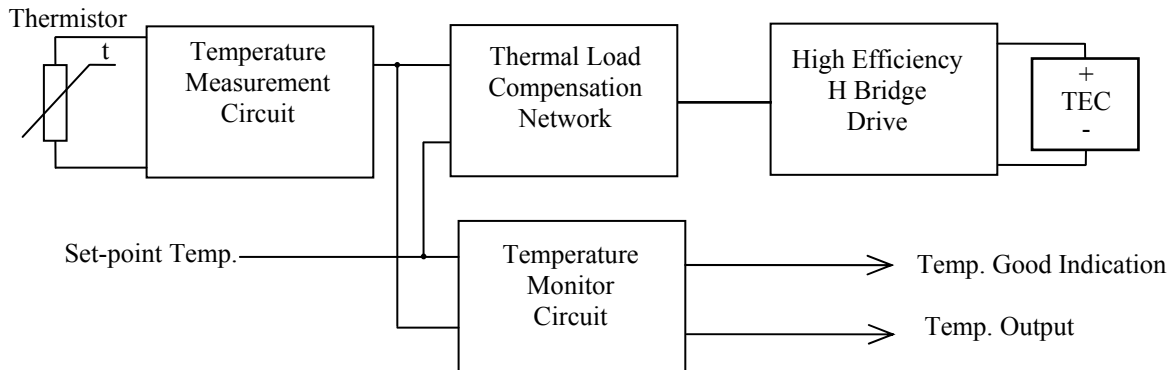


Figure 3 TEC controller block diagram

APPLICATIONS

TEC controller connections are shown in Figure 4.

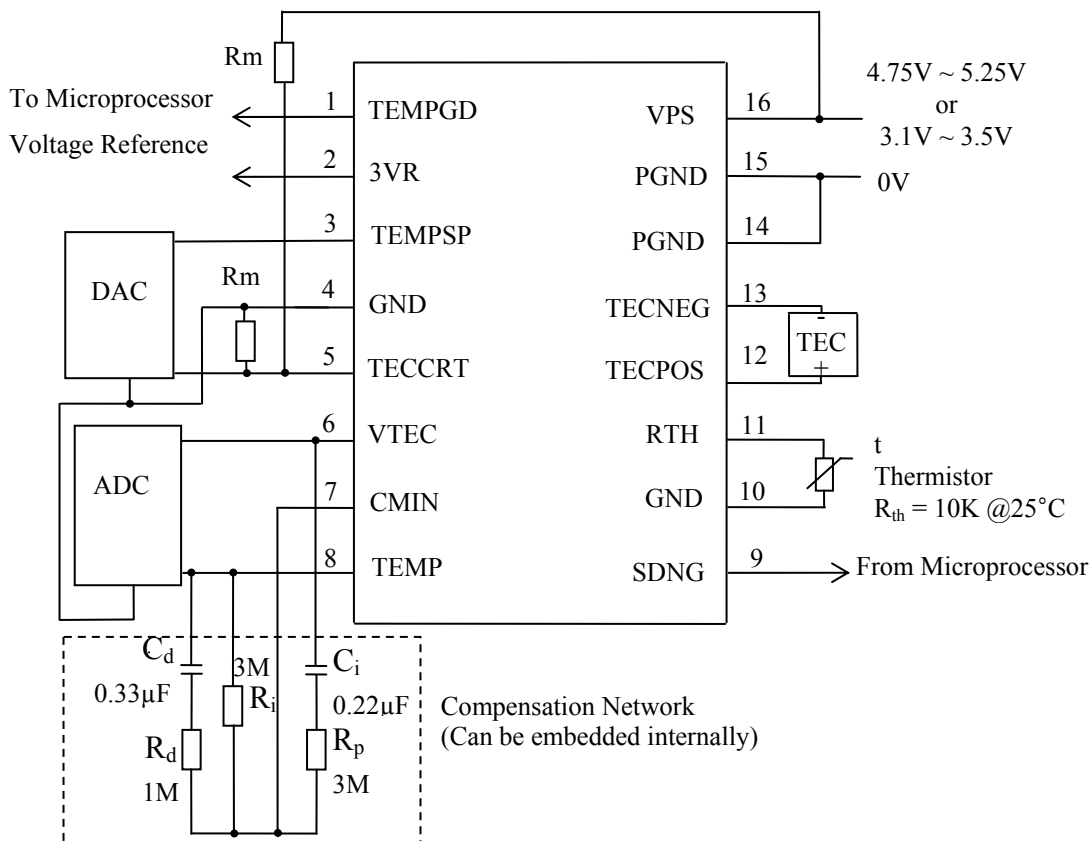


Figure 4. Microprocessor Based Application Circuit

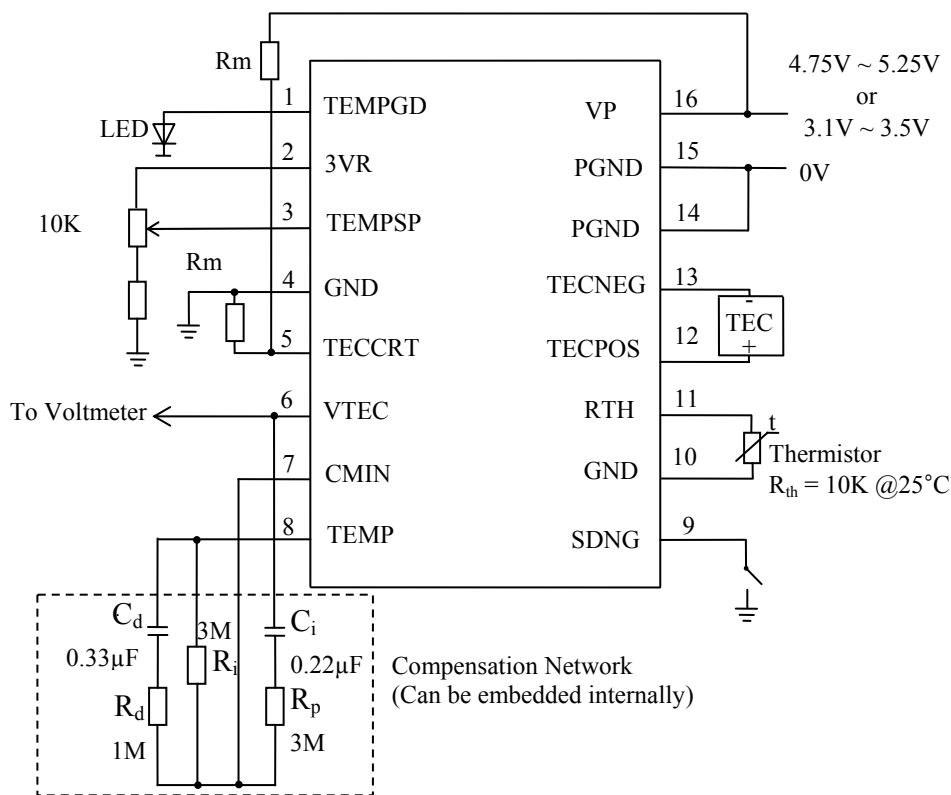


Figure 5 Stand-Alone Application Circuit

When the TEC controller is used stand-alone, using a POT or a pair of resistors to replace the POT to set the voltage for the set-point temperature pin TEMPSP as shown in Figure 3. The input voltage range on the TEMPSP pin must be $>0.1V$ and the maximum voltage on this pin is $VPS - 0.1V$. The VTEC can be utilized for measuring the voltage across the TEC as described in Table 2. The actual object temperature can be monitored by measuring the voltage on the TEMP pin. The relationship between the actual temperature and the TEMP voltage is determined by the internal temperature network. When using the default temperature network, the relationship is shown in Figure 5, the approximate formula is:

$$\beta = \log_{10}(R_0 T_1 / R_0 T_2) / [(1/T_1 - 1/T_2) \times \log_{10} e]$$

$R_0 T_1$ stands for the zero power resistance at absolute temperature T_1

$R_0 T_2$ stands for the zero power resistance at absolute temperature T_2

T_1 is the temperature 1, expressed in degree Kelvin

T_2 is the temperature 2, expressed in degree Kelvin

The maximum error between the actual output voltage and the approximated voltage is 0.013V, equivalent to 1.3% error.

If this TEC controller is to be used for other applications not discussed here, such as use it with wave locker controllers, please consult with us and we can help. The same as to other customizations, such as setting the **TEMPSP** by using a voltage source swinging above 3V and/or VPS. The TECA1-XV-XV-D controller comes with a default temperature setting network, it sets the set-point temperature to be between 15°C to 35°C when setting the TEMPSP pin voltage to be between 0V to 3V linearly and using a specific de-facto “standard” 10K @ 25°C thermistor, with its R-T value data listed in Figure 6 and Table 3. When using different thermistors and/or needing different set-point temperature ranges, please contact us, we will configure the internal temperature network for you.

When using, users need to connect the pins of VTEC and CMIN together. Connect the TEMPSP pin to DAC. About ADC, users can figure it yourself.



TYPICAL CHARACTERISTICS

Table 3 Measurement Data of Rth vs. Temperature

Temperature	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Rth	26.49	25.44	24.44	23.48	22.56	21.68	20.83	20.02	19.42	18.5	17.78	17.1	16.44	15.81	15.21	14.63	14.07
Temperature	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
Rth	13.54	13.03	12.54	12.07	11.62	11.19	10.78	10.38	10	9.635	9.286	8.95	8.629	8.32	8.024	7.74	7.746
Temperature	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
Rth	7.205	6.954	6.714	6.481	6.258	6.044	5.839	5.641	5.451	5.269	5.093	4.924	4.762	4.605	4.455	4.455	4.171

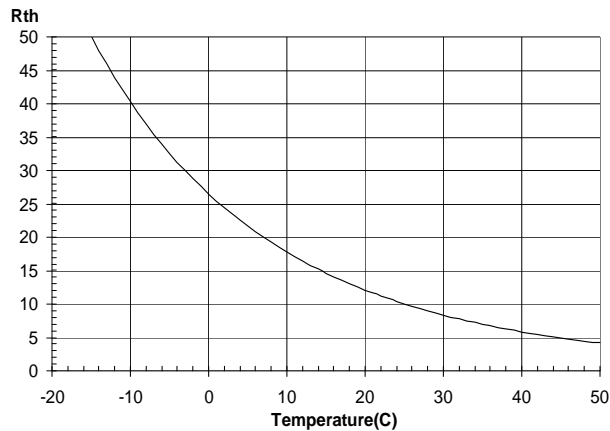


Figure 6 Rth vs. Temperature

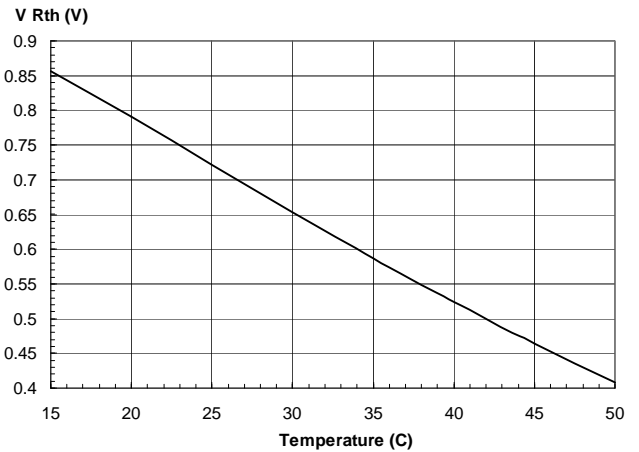


Figure 9 V_{Rth} vs. Temperature

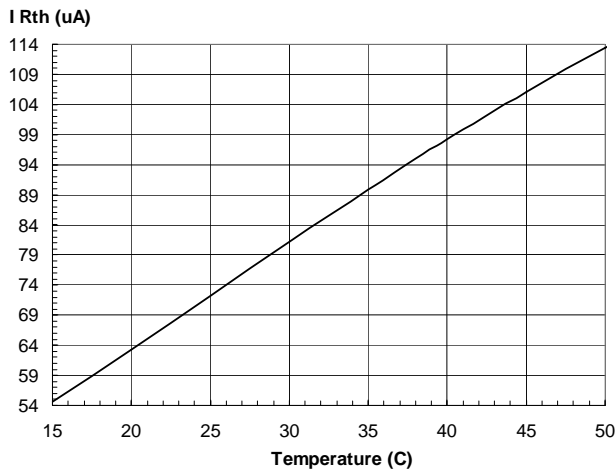


Figure 8 I_{Rth} vs. Temperature

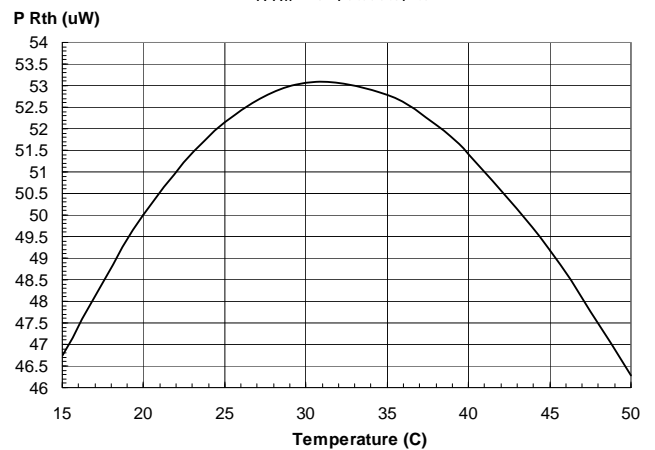


Figure 10 P_{Rth} vs. Temperature

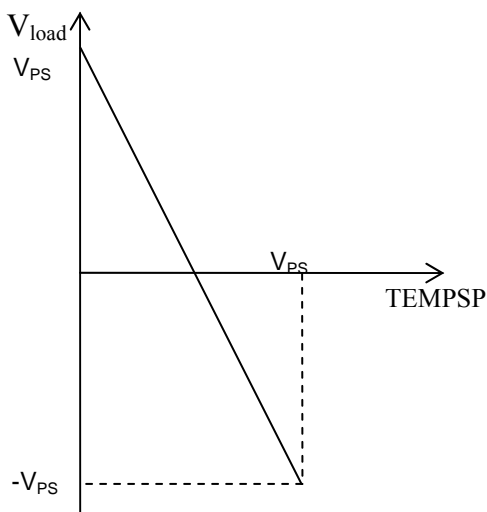


Figure 12 V_{load} vs. $TEMPSP$

Figure 12 shows the relationship between V_{load} and $TEMPSP$. With the increase of the voltage of $TEMPSP$ pin, V_{load} will decrease linearly. The approximate formula is $V_{load} = TECPOS - TECNEG$. When the $TEMPSP$ voltage reaches half of V_{PS} , V_{load} is zero; when reaches V_{PS} , the voltage will be $-V_{PS}$.

In order to conveniently show the customers the characteristics of TECA1-XV-XV-D, we offer the efficiency curves. Figure 13 show the relation between Output Voltage and Efficiency, Figure 14 shows the relation between Output Current and Efficiency.

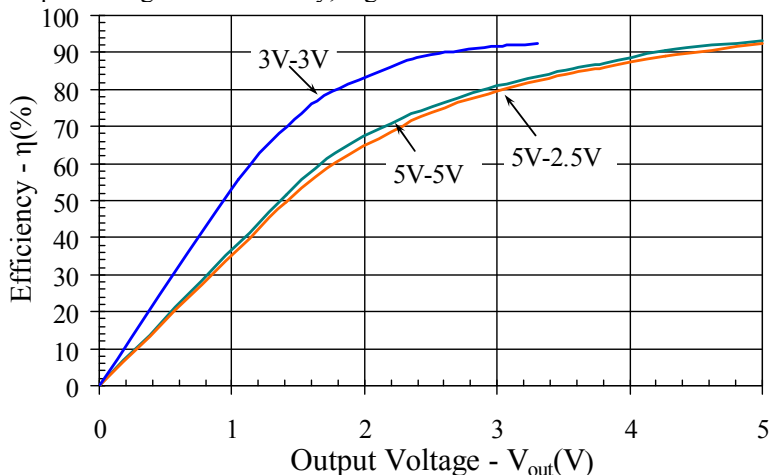


Figure 13 Efficiency vs. V_{out}

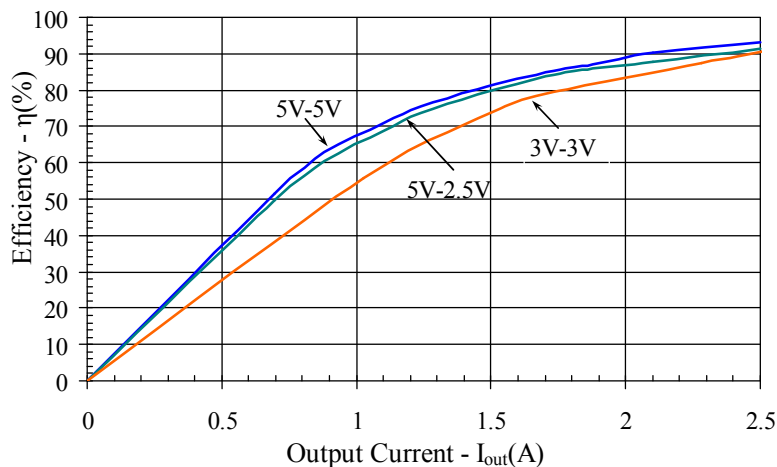


Figure 14 Efficiency vs. I_{out}



MECHANICAL DIMENSIONS

The controller comes in only one package: through hole mount. It is often called DIP (Dual Inline package) or D (short for DIP) package and has a part number: TECA1LD-XV-XV-D. Dimensions of the DIP package controller is shown in Figure 15.

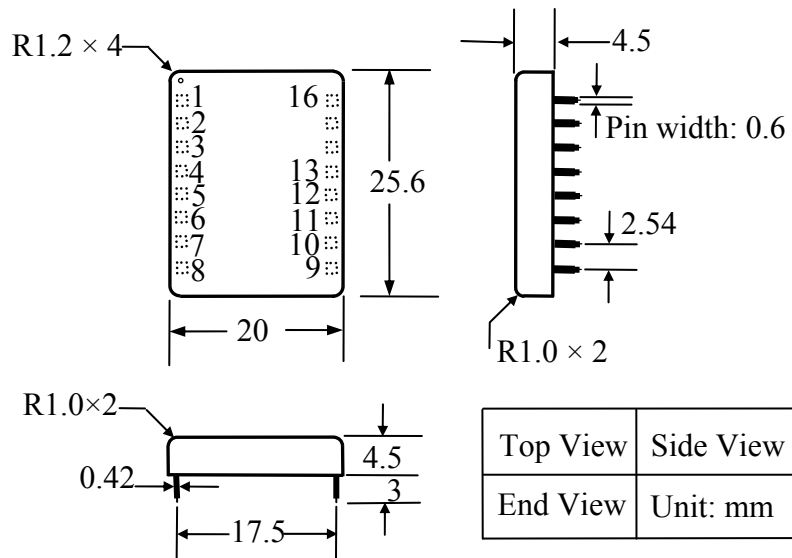


Figure 15 Dimensions of the DIP package controller of TECA1-XV-XV-D



CUSTOMIZATIONS

It is often found that some of the default specifications do not meet our users' particular need. We offer customizations on these specifications:

- 1. Maximum output voltage across TEC. When ordering, the part number will become: TECA1-5V-(max. TEC voltage)-D. E.g., TECA1-5V-2.5V-D
2. Set-point temperature range. When ordering, specify the lower limit, the upper limit, and the open circuit temperature. The part number will become: TECA1-5V-2.5V- (lower temp. limit)/(upper temp. limit)/(open circuit temp.), where lower temp. limit is the temperature corresponding to TEMPSP = 0V; upper temp. limit is the corresponding to TEMPSP = 3V; open circuit temp. corresponding to TEMPSP = 1.5V or being left unconnected. E.g., TECA1-5V-2.5V-D (20/80/50).
3. Asymmetrical maximum TEC voltage. The maximum TEC voltage for heating and cooling are not the same. When ordering, the part number will become: TECA1-5V- (max. TEC voltage for cooling/Max. TEC voltage for heating). E.g., TECA1-5V-2.5V/1.5V-D.

ORDERING INFORMATION

Table 4 Part Number

Table with 3 columns: Part Number, Description, Note. Rows include TECA1-5V-XV*-D, TECA1LD-5V-XV*-D, TECA1-3V-XV*-D, and TECA1-LD-3V-XV*-D.

*XV stands for the maximum output voltage across TEC. E.g., TECA1-5V-3.5V-D

NOTICE

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7. After many experiments, according to the parameter and the figuring method of Rload, we advice customers to use Rload of 2Ω to get the ideal character. We can also make the Maximum Output Voltage reach any value of (VPS - 0.1*Iout) if you need.